REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1, 4, 5, and 7-10 are currently pending. Claims 1, 5, 7, and 8 have been amended; and Claim 10 has been added by the present amendment. The changes and additions to the claims are supported by the originally filed specification and do not add new matter.

In the outstanding Office Action, Claims 1, 4, 5, and 8 were rejected under 35 U.S.C. § 112, second paragraph, regarding the claimed control means and storage means; Claims 1 and 8 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,794,066 to Dreyer et al. (hereinafter "the '066 patent"); Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over the '066 patent further in view of Official Notice; and Claims 5, 7, and 9 were rejected under 35 U.S.C. §103(a) as being unpatentable over the '066 patent in view of U.S. Patent No. 6,065,113 to Shiell et al. (hereinafter "the '113 patent").

Applicants wish to thank the Examiner for the interview granted Applicants' representative on July 19, 2007, at which time a proposed amendment to the claims was discussed. At the conclusion of the interview, the Examiner indicated that the claims would likely distinguish over the applied '066 patent if amended to clarify that the external device is external to and removable from the semiconductor integrated circuit.

Amended Claim 1 is directed to a semiconductor integrated circuit apparatus mounted on a predetermined circuit board, the apparatus comprising: (1) semiconductor information storage means for storing semiconductor information unique to the semiconductor integrated circuit apparatus; and (2) semiconductor information output means connected to the

semiconductor information storage means for reading out the semiconductor information from the semiconductor information storage means in response to a signal supplied by an external device that is external to, connectable to, and removable from the semiconductor circuit apparatus, the external device storing an executable program and having a predetermined non-volatile storage region, and writing the read-out semiconductor information to the predetermined storage region of the external device. Further, Claim 1 clarifies that the semiconductor information output means includes first control means, which is configured to be connected to the external device storing the executable program, for controlling a read-out operation of the program stored in the external device, the program being used for executing the read-out operation of the semiconductor information, and second control means for controlling the read-out operation and external outputting operation of the semiconductor information by executing the read-out program read by the first control means. The changes to Claim 1 are supported by the originally filed specification and do not add new matter.[1]

Applicants respectfully submit that the rejections of Claims 1, 4, 5, and 8 are rendered moot by the present amendment to those claims. Claims 1, 5, and 8 have been amended to address the antecedent basis questions noted in the outstanding Office Action. Accordingly, Applicants respectfully submit that those rejections are rendered moot.

Regarding the rejection of Claim 1, the '066 patent is directed to a method for determining microprocessor attributes in response to an ID instruction, including the steps of reading a first type of information from a processor memory element in the microprocessor in response to the ID instruction, storing at least a portion of the first type of information in at least one register in the microprocessor, and retrieving additional information from the processor memory element, if the first type of information indicates that more than one level

[1] See, e.g., Figure 3 and pages 14-16 of the specification.

of information is available. As shown in Figure 1, the '066 patent discloses that a microprocessor 10 having related software 12 includes a processor ID register 30 formed on the microprocessor 10 as a read-only register. Further, the '066 patent discloses that the register 30 includes processor ID information 31. Further, the '066 patent discloses that the software programs 12 includes a main program 50, a program for testing ID flag 18, and a CPUID instruction 54, which may be a single instruction. The '066 patent discloses that the CPUID instruction can be executed on the control unit 40 using the decoder 41, the control logic 42, and the microcode 43. Further, the '066 patent discloses that "a CPUID instruction makes information available to software to identify the microprocessor but only if it has implemented the (CPUID) instruction."[2] In addition, the ''066 patent discloses that the CPUID instruction, when executed, executes a microcode sequence to read the contents of the processor ID 30 and to store them in a general purpose register such as the first general purpose register 20 or the second general purpose register 22.[3]

However, Applicants respectfully submit that the '066 patent fails to disclose a semiconductor integrated circuit apparatus mounted on a predetermined circuit board that includes semiconductor information output means for reading out the semiconductor information from the semiconductor information storage means in response to a signal supplied by an external device that is external to, connectable to, and removable from the semiconductor circuit apparatus, the external device storing an executable program and having a predetermined non-volatile storage region, wherein the semiconductor information output means also writes the read-out information to the predetermined storage region of the external device, as recited in Claim 1. The '066 patent does not disclose that the program for executing the read-out operation of the semiconductor information is stored on an external

[2] The '066 patent, column 12, lines 58-60.
[3] See '066 patent, column 6, lines 44-52.

device external to and removable from the semiconductor integrated circuit and that the read-out information is written into a predetermined storage region on the external device. Rather, the '066 patent merely discloses that the processor 10 has associated software 12 that includes a CPUID instruction that can be executed on the microprocessor. The '066 patent does not disclose an external device having an executable program and a predetermined storage region in which the semiconductor information read-out by the program stored on the external device is then stored in the predetermined non-volatile storage region of the external device, as required by Claim 1. Accordingly, Applicants respectfully submit that the rejection of Claim 1 as anticipated by the '066 patent is rendered moot by the present amendment to Claim 1.

Independent Claim 8 recites limitations analogous to the limitations recited in Claim 1. Moreover, Claim 8 has been amended in a manner analogous to the amendment to Claim 1. Accordingly, for reasons analogous to the reasons stated above for the patentability of Claim 1, Applicants respectfully submit that the rejection of Claim 8 is rendered moot by the present amendment to Claim 8.

Claim 5 is directed to a circuit board on which a semiconductor integrated circuit apparatus is mounted, the circuit board comprising: (1) semiconductor information storage means for storing semiconductor information unique to the semiconductor information circuit apparatus; and (2) semiconductor information output means, which is configured to be connected to the semiconductor information storage means, for reading out the semiconductor information from the semiconductor information storage means in response to a signal supplied by an external device that is external to, connectable to, and removable from the semiconductor integrated circuit apparatus, the external device storing an executable program and having a predetermined non-volatile storage region, and writing the read-out

semiconductor information to the predetermined storage region of the external device. Further, Claim 5 clarifies that the external device stores the executable program being used for executing the read-out operation of the semiconductor information, and the semiconductor information output means controls the read-out operation of the semiconductor information by executing the program read out from the external device, and the write-in operation of the semiconductor information to the external device. The changes to Claim 5 are supported by the originally filed specification and do not add new matter.

Regarding the rejection of Claim 5 under 35 U.S.C. §103, the Office Action asserts that the '066 patent discloses everything in Claim 5 with the exception of writing the semiconductor information to the storage means storing the read-out program, and relies on the '113 patent to remedy that deficiency.

As discussed above, the '066 patent is directed to a method for determining microprocessor attributes in response to an ID instruction. However, as admitted in the outstanding Office Action, the '066 patent fails to disclose a semiconductor information output means that writes the read-out semiconductor information into a storage means. Further, Applicants respectfully submit that the '066 patent fails to disclose a circuit board including a semiconductor information output means for reading-out semiconductor information from a semiconductor information storage means in response to a signal supplied by an external device that is external to, connectable to, and removable from the semiconductor integrated circuit apparatus, the external device storing an executable program and having a predetermined non-volatile storage region, and for writing the read-out semiconductor information into the predetermined region of the external device, as recited in amended Claim 5.

The '113 patent is directed to a method of operating a microprocessor including the steps of storing an identifier code uniquely identifying the microprocessor in a one-time programmable register in the microprocessor, issuing to the microprocessor an identifier request instruction from the instruction set, and in response to the identifier request instruction, reading from the one-time programmable register of the microprocessor the identifier code. As shown in Figure 1, the '113 patent discloses that, in step 18, the method outputs the microprocessor identifier code. Further, the '113 patent discloses that this information "may be used internally for further processing by the microprocessor, or may be output externally for use by features such as those set forth above (i.e., BIOS, operating system, application program)."[4]

However, Applicants respectfully submit that the '113 patent fails to disclose a semiconductor information output means that writes the read-out semiconductor information to a predetermined non-volatile storage region of an external device, as recited in Claim 5. Rather, the '113 patent merely discloses that microprocessor information may be output externally from the microprocessor for use by the operating system or an application program. The '113 patent does not teach or suggest an external device having a predetermined non-volatile storage region in which the semiconductor information is written to, as recited in amended Claim 5.

Thus, no matter how the teachings of the '066 and '113 patents are combined, the combination does not teach or suggest semiconductor information output means for reading out semiconductor information from the semiconductor information storage means in response to a signal supplied by an external device that is external to, connectable to, and removable from the semiconductor circuit apparatus, the external device storing an executable program and having a predetermined non-volatile storage region in which the

[4] See the '113 patent, column 3, lines 36-39.

read-out storage information is stored. Accordingly, Applicants respectfully submit that the rejection of Claim 5 is rendered moot by the present amendment to Claim 5.

Independent Claim 7 recites limitations analogous to the limitations recited in Claim 5. Moreover, Claim 7 has been amended in a manner analogous to the amendment to Claim 5. Accordingly, for reasons analogous to the reasons stated above for the patentability of Claim 5, Applicants respectfully submit that the rejection of Claim 7 is rendered moot by the present amendment to that claim.

Regarding the rejection of dependent Claim 4 under 35 U.S.C. §103, Applicants respectfully submit that the Official Notice taken in the Office Action fails to remedy the deficiencies of the '066 patent. Accordingly, Applicants respectfully submit that the rejection of dependent Claim 4 is rendered moot by the present amendment to Claim 1. Moreover, Applicants request that a reference be cited to support the Official Notice taken by the Office.

The present amendment also sets forth new Claim 10 for examination on the merits. New Claim 10 clarifies that the external device is one of a flash memory device and a compact disc. Claim 10 is supported by the originally filed specification and does not add new matter.[5]

Thus, it is respectfully submitted that independent Claims 1, 5, 7, and 8 (and all associated dependent claims) patentably define over any proper combination of the '066 patent, the '113 patent, and Official Notice.

[5] See page 15 of the specification.

Consequently, in view of the present amendment and in light of the above discussion, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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